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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,134	11/15/2001	Linden Minnick	042390P12310	6022

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EXAMINER	
TRUONG, LECHI	

ART UNIT	PAPER NUMBER
2194	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/003,134	MINNICK ET AL.	
	Examiner	Art Unit	
	LeChi Truong	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3-4, 6-12, 14-23, 25- 28, 30-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-4, 6-12, 14-23, 25- 28, 30-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/29/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-4, 6-12, 14-23, 25- 28, 30-48 are presented for examination. Claims 2, 5, 13, 24, 29 are canceled.

Claim Rejections - 35 USC § 112

2. Claims 37, 40, 45, and 48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to claims 37, 40, 45, 48, the claims contain the subject matter "writing a second completion status to a memory address occur prior to writing a first completion status wherein execution of a command in the first descriptor is initialed before execution of a command in the second descriptor is initialed" was not described in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,11, **12, 16, 17, 23, 28, 33, 34, 36, 37, 39-40, 44, 45, 47, 48** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) and further in view Bonevento et al (US. Patent 5,131082).

As to claim 1, Harrington teaches the invention substantially as claimed including: a plurality of operation descriptors (corresponding blocks/list of command sequences, col 2, ln 15-20/ control block lists, col 18, ln 49-55), a controller (I/O controller, col 2, ln 15-20), issuing a plurality of commands to a controller, wherein the operational descriptors are issued in a first order (corresponding blocks or lists of command sequences, appropriate commands of each sequence are stored in the I/O controller local memory at any one time for suitable execution, col 2, ln 15-20/col 4, ln 18-22/ ln 42-46), each operating descriptor includes a command(col 18, ln 49-53), indicating the completion status of commands is indicated in a second order (Once a complete sequence of commands from any control block list has been performed, the requester 15 provide return information to the host CPU notifying the latter the such sequence has been completed and proving suitable status information concerning the state, col 4, ln49-55), the term the second order is capable of being different from the first order (the commands are issued to the controller for execution at the same time[first order], col 2, ln 15-20/col 4, ln 18-22/ ln 42-46, . After completed the execution of all the commands, the indication for the completion of commands is provided [the second order], col 4, ln49-55).

Harrington do not explicitly teaches a receiving a plurality descriptors at a controller, descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the commend will be written upon completion of

the command, upon completion of a command includes in a respective descriptor, writing a completion status value for the command address external to the respective descriptor. However, Bonevento teaches a plurality descriptors at a controller, descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the commend will be written upon completion of the command, upon completion of a command includes in a respective descriptor, writing a completion status value for the command address external to the respective descriptor (transmit commands in the form of system Control Blocks (SCB's) between a host system and a plurality of subsystems, col 2, ln 24-26/ provides an immediate command or the address of a subsystem control block(SCB) to at least one subsystem, col 2, ln 59-63/ the chaining of SCB commands allows the intelligent subsystem to fetch and execute commands, col 3, ln 50-54/ Each SCB includes the address of a Termination Status Block(TSB) in system memory, to which the subsystem which is processing the SCB stores completion or termination status for the SCB, col 3, ln 55-58/ A SCB includes the address of a Termination Status Block(TSB) in system memory. The completion or termination status of a given SCB is placed in the TSB by the subsystem processing the command. In order to handle termination at any point in a chain command, col 5, ln 49-54/ Status of completion or terminal for the SCB is stored into TSB 214, col 19, ln 34-36).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Harrington to incorporate the feature of the descriptor includes a command and a memory address identifying a memory location external to the descriptor to which a completion status of the commend will be written upon completion of the

command because this ensures the integrity of an entire system without the need to use a priority interrupt or other machine to report immediate status to the host program.

As to claim 11, Harrington teaches the value to be written indicated the command's original location (col 11, ln 60-65).

As to claim 12, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Harrington teaches a machine –readable medium having instruction (col 3, ln 10-15).

As to claims 16, 17, they are apparatus claims of claims 11, 5; therefore, they are rejected for the same reasons as claims 11, 5 above.

As to claim 23, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above.

As to claim 28, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above. In additional, Harrington teaches a plurality of computation units (col 4, ln 6-9).

As to claim 33, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim above. In additional, Harrington teaches executing the commands in a first order (corresponding blocks or lists of command sequences, appropriate commands of each sequence are stored in the I/O controller local memory at any one time for suitable execution, col 2, ln 15-20/ the host execute the commands in an established sequence, col 4, ln 4, ln 42-44/ Once a complete sequence of commands from any control bocks has been performed [first order], the register 15 provide return information for the host CPU notifying the latter that such sequence has been completed[second order], col 4, ln 49-55).

As to claim 34, it is an apparatus claim of claim 1; therefore, it is rejected for the same reason as claim 1 above.

As to claim 36, Bonevento teaches at least some of the descriptor comprises a value to be written to the memory address identifying a memory location external to the descriptor upon completion of the command or the descriptor (col 15, ln 39-43, col 60-67/col 17, ln 5-15/ ln 19-23).

As to claim 37, Bonevento teaches writing a second completion status to a memory address external to a second descriptor occurs prior to writing a first completion status to a memory external to a first descriptor; and execution of a command in the first descriptor in initiated before execution of a command in the second descriptor (col 5, ln 49-54/ col 9, ln 33-37)).

As to claim 39-40, 44, 45, 47, 48, they are apparatus claims of claims 36, 37; therefore, they are rejected for the same reasons as claims 36, 37 above.

4. Claims **3, 4, 14, 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Bonevento et al (US 5,131082) and further in view of Kohn (US. Patent 4,366,536).

As to claims 3, 4, Harrington and Bonevento do not teach an absolute address and an offset from a base memory address. However, Kohn teaches an absolute address and an offset from a base memory address (address indicated the offset; the absolute variable data are addresses, col 2, ln 8-16/ ln 42-45).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Bonevento and Kohn because Kohn's address indicated the offset, the absolute variable data are addresses would improve the efficiency of Harrington and Bonevento's systems by providing addresses to the respective memories and the program counter to the respective memories to make the i/o system more consistent.

As to claims 14, 15, they are apparatus claims of claims 3, 4; therefore, they are rejected for the same reasons as claims 3, 4 above.

5. Claims **6-9, 18-21, 25-26, 30-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Bonevento et al (US 5,131082), as applied to claim 1 above, and further in view of Saito (US. Patent 6,567,862 B1).

As to claim 6, Harrington and Bonevento do not teach the commands are grouped into categories. However, Saito teaches the commands are grouped into categories (groups received commands and stored commends to predetermined command group are according to group, col 2, ln 28-35).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Bonevento and Saito because Saito's groups received commands and stored commends to predetermined command group are according to group would improve the flexibility of Harrington, Bonevento's systems by allowing movement of a recording head of the data server to be reduced. Therefore, the efficiency of disk access could be improved.

As to claims 7, 8, 9, Saito teaches their execution time/ a plurality of resource executes / a plurality of memory location (according to a recording area on the data recording medium accessed by each command, col 3, ln 1-5/based on this address information... corresponding to the access disk, col 8, ln 45-56/ at the command execution time T', col 12, ln 41-42).

As to claims 18-21, 25-26, 30-31, they are apparatus claims of claims 6-9; therefore, they are rejected for the same reasons as claims 6-9 above.

6. Claims **10, 22, 27, 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) in view of Bonevento et al (US 5,131082), as applied to claim 1 above, in view of Saito (US. Patent 6,567,862 B1) and further in view of Ghaffari et al (US. Patent 6,088,740).

As to claim 10, Harrington, Bonevento and Saito do not teaches a single memory location. However, Ghaffari teaches a single memory location (a set of n command blocks 210-211, col 4, and ln 4-10).

I would have been obvious to one of the ordinary skill in the art at the time the invention was made to combine the teaching of Harrington, Bonevento, Saito and Ghaffari because Ghaffari's a single memory location improve the reliability of Harrington, Bonevento, and Saito's systems by executing discrete commands quickly and efficiently for an error recovery when necessary.

As to claims 22, 27, 32, they are apparatus claims of claim 10; therefore, they are rejected for the same reason as claim 10 above.

7. Claims **35, 38, 41, 42, 43, 46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington et al (US. Patent 4,939,644) and further in view Bonevento et al (US. Patent 5,131082) and further in view of Kusakabe et al (6,073 236).

As to claim 35, Harrington and Bonevento do not teach at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms. However, Kusakabe teaches at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms (receive a command from the R/W 1 from a decryption section 83 (decryption means), perform a process corresponding to command, and outputs response data (to be transmitted to encryption section 82(encryption means), col 6, ln 32-56/ col 10, ln 52-57/ col 11, ln 5-13).

It would have been obvious to one of the ordinary skill in the art at the time the invention was made to modify the teaching of Harrington and Bonevento to incorporate the feature of at least some of the descriptors comprise commands executed by one of multiple encryption units implementing different respective encryption algorithms because this allows two information processing which have authenticated each other to perform communications.

As to claims 38, 41, 42, 46. they are apparatus claims of claim 35; therefore, they are rejected for the same reason as claim 35 above.

As to claim 43, Kusakabe teaches data Encrytion Standard (col 1, ln 38-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LeChi Truong whose telephone number is (571) 272 3767. The examiner can normally be reached on 8 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomson, William can be reached on (571) 272 3718. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR of Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

LeChi Truong

November 21, 2006

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER